WT-QSFP28-SR4
100Gbs QSFP28 SR4 Optical Transceiver Module

1. Features

- Four-channel full-duplex transceiver modules
- Transmission data rate up to 25.78125Gbit/s per channel
- Up to 100m on OM4 Multimode Fiber (MMF)and 100m on OM4 MMF
- Low power consumption <2.5W
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant
- Hot Pluggable QSFP form factor
- MPO connector receptacle
- Built-in digital diagnostic function

2. Applications

- IEEE 802.3bm 100GBASE SR4 and 40GBASE SR4
- Proprietary High Speed Interconnections
- Data center

3. Description

The Wintop WT-QSFP28-SR4 is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP28 Transceiver for IEEE 802.3bm, 100GBASE SR4 Applications， or 40 Gigabit Ethernet and Infiniband FDR/EDR Applications. The QSFP28 full-duplex optical module offers 4 independent transmit and receive channels, each capable of 25.78125 Gbps operation for an aggregate data rate of 104Gbps 70m using OM3 fiber. These modules are designed to operate over multimode fiber systems using 850nm VCSEL laser array. An

optical fiber ribbon cable with an MPO/MTP™ connector can be plugged into the QSFP module receptacle. QSFP28 SR4 is one kind of parallel transceiver which provides increased port density and total system cost savings.

4. Absolute Maximum Ratings

The operation in excess of any absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	TST	-40	85	℃	
Relative Humidity(non-condensing)	RH	0	85	%	
Operating Case Temperature	TOPC	0	70	℃	

Supply Voltage	VCC	-0.3	3.6	V	
Input Voltage	Vin	-0.3	Vcc+0.3	V	

5. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	TOPC	0		70	℃
Power Supply Voltage	VCC	3.13	3.3	3.47	V
Power Consumption		-		2.5	W
Data Rate	DR		25.78125		Gbps
Data Speed Tolerance	ΔDR	-100		+100	ppm
Link Distance with OM4 fiber	D			100	m

6. Optical Characteristics

All parameters are specified under the recommended operating conditions with PRBS31 data pattern unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Center Wavelength	λC	830		870	nm	1
RMS Spectral Width	λrms	-		0.65	nm	1
Average Launch Power, each lane	PAVG	-8.4		2.4	dBm	
Optical Modulation Amplitude (OMA)	POMA	-5		3	dBm	1
Difference in Launch Power between any two lanes	Ptx,diff			4.0	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane	OMA-TDP			3.5	dB	1
Extinction Ratio	ER	3			dB	
Transmitter Eye Mask Margin	EMM	10			%	2
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}					
Receiver						
Center Wavelength	λC	820		880	nm	
Damage Threshold	THd	+3			dBm	
Overload, each lane	OVL	+2.4			dBm	
Receiver Sensitivity in OMA, each Lane@BER 5E-5	SEN			-10.3	dBm	
Signal Loss Assert Threshold	LOSA	-30			dBm	
Signal Loss Deassert	LOSD			-12	dBm	

Threshold						
LOS Hysteresis	LOSH	0.5		6	dB	
Optical Return Loss	ORL			-12	dBm	

Notes:

Transmitter wavelength, RMS spectral width and power need to meet the OMA minus TDP specs to guarantee link performance.

The eye diagram is tested with 1000 waveform.

7. Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential input voltage amplitude	ΔVin	300		1100	mVp-p
Differential Output impedance	Zout	90	100	110	ohm
Differential output voltage amplitude	ΔVout	500		800	mVp-p
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

8. Pin Descriptions

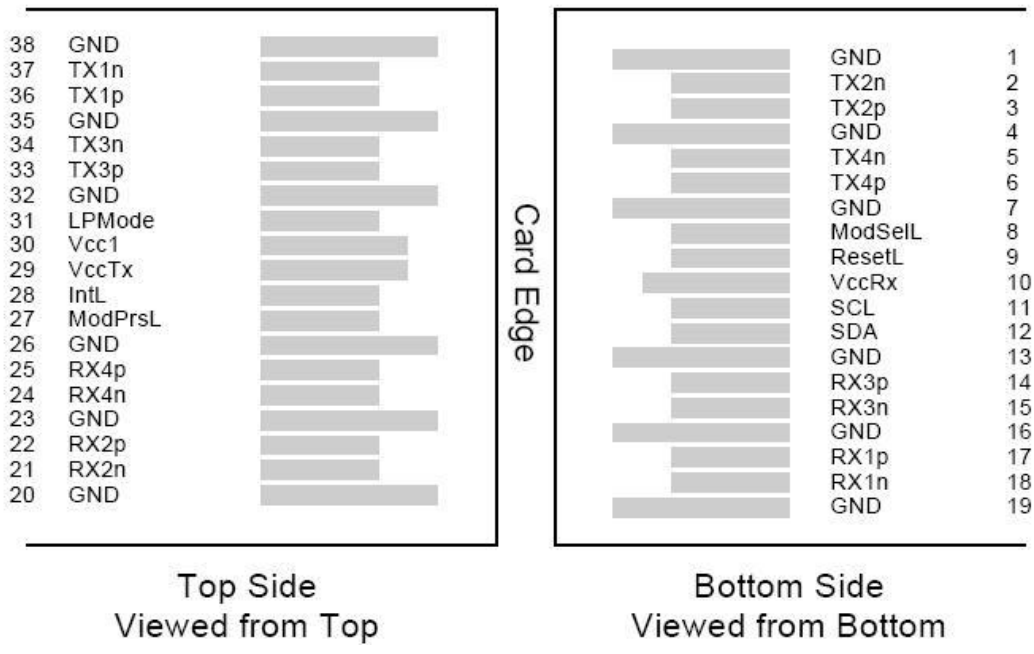
PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	

18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

Module circuit ground is isolated from module chassis ground within the module. GND is the symbol for signal and supply (power) common for QSFP modules.

The connector pins are each rated for a maximum current of 500mA.



ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Wintop QSFP28 SR4 operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

9. Power Supply Filtering

The host board should use the power supply filtering shown in Figure 1.

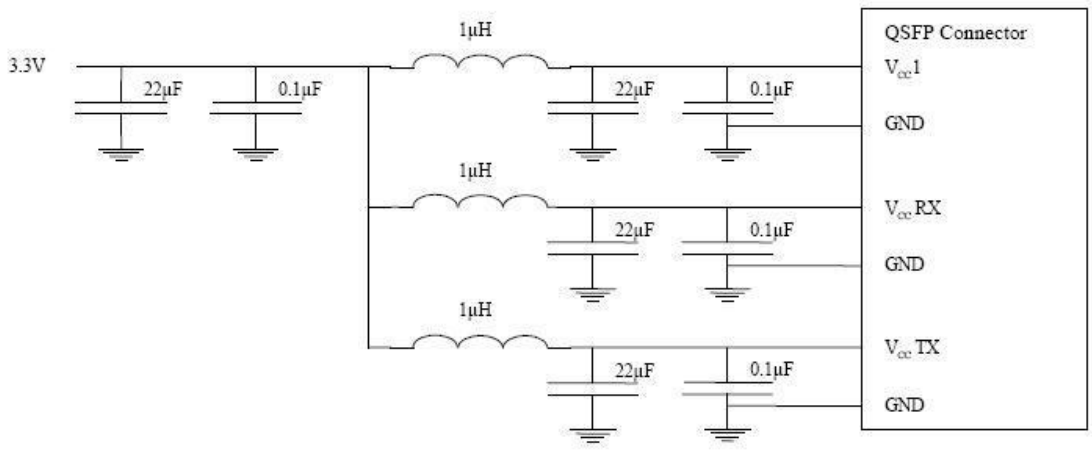


Figure1. Host Board Power Supply Filtering

10. Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector .The four fiber positions on the left as shown in Figure 2, with the key up, are used for the optical transmit signals (Channel 1

through4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.

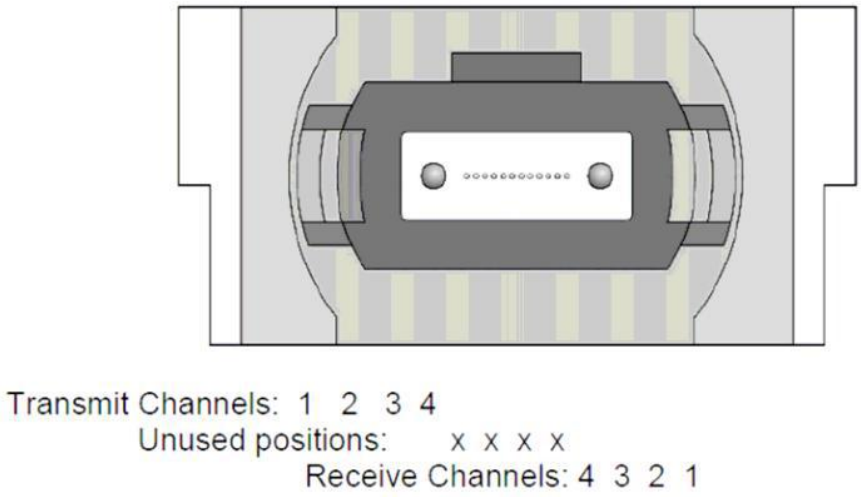


Figure 2. Optical Receptacle and Channel Orientation

11. Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all WINTOP QSFP28 SR4. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in Figure 3. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Parameter	Symbol	Min.	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-3	3	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%	10%	mA	Per channel

12. Mechanical Dimensions